Listing of Claims:

1. (Previously presented) A computer system, comprising:

a processor;

a system memory coupled to said processor;

a bridge logic device coupled to said processor and said system memory and having a peripheral bus interface, wherein said bridge logic device is associated with at least a first address line;

a peripheral bus comprising a plurality of address lines, including the first address line, and coupled to the peripheral bus interface of said bridge logic device, said peripheral bus capable of coupling together various peripheral devices;

a first peripheral device coupled to said peripheral bus, wherein said first peripheral device is associated with said first address line;

an input/output device coupled to said bridge logic device; and

a logic device coupled to said peripheral bus that swaps a second address line for said first address line when a peripheral bus cycle is run to said first address line.

2. (Original) The computer system of claim 1 wherein said peripheral bus comprises a PCI bus.

3. (Original) The computer system of claim 1 wherein said logic device comprises a PLD.

4. (Previously presented) The computer system of claim 1 wherein said logic device swaps the second address line for said first address line when a peripheral bus configuration cycle is run.

5. (Previously presented) The computer system of claim 4 wherein said logic device issues a retry to said bridge logic which, in response, issues a retry to said processor.

6. (Previously presented) The computer system of claim 4 wherein said peripheral bus comprises a PCI bus including said first address line and said second address line and said logic device is a programmable logic device that detects a PCI configuration cycle run for one of the address lines comprising the PCI bus.

7. (Previously presented) The computer system of claim 6 further comprising an electronically controlled switch coupled to and controlled by said programmable logic device, said switch receiving at least two PCI bus address lines.

8. (Previously presented) The computer system of claim 6 wherein said programmable logic device switches the two PCI bus address lines when the programmable logic device detects a PCI bus configuration cycle targeted for one of the two address lines so that the address line targeted by the PCI bus configuration cycle is electrically connected to the other of said two address lines.

9. (Original) The computer system of claim 7 further including a PCI device connected to said PCI bus that has its IDSEL input pin connected to one of said two address lines.

10. (Cancelled).

11. (Previously presented) A programmable logic device coupled to a system bus comprising a plurality of address lines, said programmable logic device having logic that detects configuration read or write cycle to a particular system bus address line associated with a bridge logic device and, upon detecting a configuration read or write cycle to that particular address line, the programmable logic device asserts a control signal to an electronically-controlled switch to connect the particular system bus address line to another address line.

12.-13. (Cancelled).

14. (Original) The programmable logic device of claim 11 wherein programmable logic device issues a retry signal upon detecting the configuration read or write cycle to the said particular address line.

15.-22. (Cancelled).

23. (Previously presented) A computer system, comprising:

a processor;

a bridge logic device coupled to said processor and a system bus that comprises a plurality of address lines including a first address line;

at least one system bus peripheral device connected to said system bus, wherein said at least one system bus peripheral device is associated with said first address line;

an electronically-controlled switch connected to at least said first address line; and

a means for detecting a system bus configuration cycle associated with a said first address line and, upon detecting the configuration cycle associated with said first address line, asserting a control signal to said switch to connect said first address line to another of the system bus address lines associated with said first peripheral device.